PVP 12

Code: **CSCS1T3**

I M.Tech - I Semester – Regular/Supplementary Examinations – January - 2017

COMPUTER ORGANIZATION AND ARCHITECTURE
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

Answer any FIVE questions. All questions carry equal marks

1. a) Explain signed 2's complement addition and subtraction. 6 M

   b) Draw the logic diagram to detect overflow in binary addition. 4 M

   c) Explain Demorgans theorem and Distributive law. 4 M

2. a) Construct Full Adder using Multiplexer. 8 M

   b) What is JK Flip flop? Explain Race condition in JK Flip flop. 6 M

3. a) What will be the size of address bus and data bus when a 4GB RAM is employed in a 32 bit computer 6 M

   b) Explain Memory Hierarchy in detail. 8 M

4. a) Explain difference between software and hardware interrupts with example. 7 M

b) Discuss various modes of Input Output transfer. 7 M

5. a) Explain multiplication algorithm with example. 8 M

b) How to detect division overflow? 6 M

6. a) Explain Register organization in Intel x86 processor family. 7 M

b) What is pipelining? Discuss instruction of pipelining. 7 M

7. a) Discuss characteristics of RISC processors. 6 M

b) What is compiler based register optimization? Explain in detail. 8 M

8. a) Multicore Organization improves performance of processor. Justify? 6 M

b) What is cache coherence? 4 M

c) What is symmetric multiprocessor architecture? 4 M